

grammatical errors, and not for any reasons related to patentability. Claims 5-9 are pending in this application.

With regard to the rejections of claims 5-9, Applicant respectfully submits that the Examiner's assertions as to certain combinations of the cited prior art do not establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103(a). It appears that the Examiner has improperly pieced various aspects of the present method invention from the prior art together with a good deal of hindsight and with the invention as a road map to make an obviousness rejection.

Applicant respectfully urges that such allegations do not establish a proper *prima facie* case of obviousness under 35 U.S.C. § 103(a). "The examiner bears the initial burden, on review of the prior art on any other ground, of presenting a *prima facie* case of unpatentability." In re Oetiker, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992) (Emphasis original). Among the criteria the Examiner must follow to establish a *prima facie* case of obviousness is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. M.P.E.P. § 2143.

Furthermore, the teaching or suggestion to make the claimed combination must be found in the prior art, not in Applicant's disclosure. In Re Vaeck, 947 F.2d 488, 493, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991). Additionally, the evidence of a teaching, suggestion, or motivation to combine must be "clear and particular." In Re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999). As will be described below, combining the cited references is improper because the required motivation is absent.

Claim 5 recites, among other things "adding boron to said second insulating layer." In rejecting this claim as being unpatentable over Zhao in view of Moore and further in view of Fraser, the Examiner asserts on Page 4 of the Office Action that "it would have been obvious for a person of ordinary skill in the art to use two materials having the same function to perform the same." First, Applicant asserts that this is a conclusory statement that is neither supported in the cited prior art, nor "clear and particular," and thus constitutes an improper basis for rejection under 35 U.S.C.

§ 103(a). Second, Applicant asserts that this proposed combination goes against the teachings of both Zhao and Fraser. Zhao discloses the deposition of SiO<sub>2</sub> over the low-k dielectric ILD layer using a CVD process. Zhao then goes on to disclose that "it is important that the material selected for the etch-stop layer 15 is different from that comprising the separation layer 13." (Col. 6, lines 23-36; emphasis added). Fraser discloses the use of "a nonmetallic material (such as the aforementioned silicon dioxide, or boron nitride or silicon nitride or glass) be utilized for the intermediate masking layer." (Col. 7, lines 34-37; emphasis added). In both references, the material to form the etch stop/intermediate masking layer is referred to in the *singular*. Thus, while Zhao and Fraser may suggest using boron nitride as a *substitute* for silicon dioxide or silicon nitride in forming the etch-stop/intermediate masking layer, neither reference suggests, and in fact they teach away, from *adding* boron nitride, or any other boron compound, to a etch-stop/intermediate masking layer made of another material. For at least these reasons, Applicant submits that independent claim 5, and its dependent claims 6-9, are allowable.

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Applicant respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 5-9 in condition for allowance. Applicant submits that this Amendment does not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicant respectfully points out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment would allow the Applicant to reply to the final rejections and place the application in condition for allowance.

Finally, Applicant submits that the entry of this Amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

In view of the foregoing remarks, Applicant submits that this claimed invention is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicant therefore requests the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

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Respectfully submitted,

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Dated: March 5, 2003

By: \_\_\_\_\_

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*substitute sheet follows.*

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APPENDIX TO AMENDMENT OF MARCH 5, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

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**AMENDMENTS TO THE SPECIFICATION**

Please replace the paragraph bridging pages 1-2 with the following:

In a deposition system shown in FIG. 10 [9], a microwave of 2.45 GHz is first supplied into a plasma producing chamber 801a from a high-frequency power supply part 802 via a waveguide 802a. At this time, a magnetic field of 875 gaussses is applied by magnetic coils 803 and 803a, and Ar gas introduced from an introducing pipe 804 is activated as a high-density plasma by the electrion cyclotron resonance.

**AMENDMENTS TO THE CLAIMS**

5. (Amended) A method of manufacturing a semiconductor device<sub>1</sub> [as set forth in claim 4, which further comprises a step of] said method comprising the steps of:

forming a wiring layer on a semiconductor substrate having an active region formed thereon;

forming a first insulating layer containing carbon on said wiring layer;

forming a second insulating layer comprising silicon, carbon and nitrogen on said first insulating layer;

adding boron to said second insulating layer;

selectively etching said second insulating layer until the surface of said first insulating layer is partially exposed;

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selectively etching said first insulating layer with plasma, using said selectively-etched second insulating layer as a mask pattern; and  
forming a new wiring layer on said second insulating layer after selectively etching said first insulating layer.

6. (Amended) [A] The method of manufacturing a semiconductor device as set forth in claim [4 or] 5, wherein said step of selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and fluorine.

7. (Amended) [A] The method of manufacturing a semiconductor device as set forth in claim [4 or] 5, wherein said step of selectively etching said second insulating layer is carried out with the plasma of the gas of a compound containing carbon and hydrogen.

8. (Amended) [A] The method of manufacturing a semiconductor device as set forth in claim [4 or] 5, wherein said step of selectively etching said second insulating layer is carried out with the plasma of an oxygen-containing gas.

9. (Amended) [A] The method of manufacturing a semiconductor device as set forth in claim [4 or] 5, wherein said step of selectively etching said second insulating layer is carried out with the plasma of a hydrogen-containing gas.

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